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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,911	04/18/2001	Hui Wang	495152000111	9922

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EXAMINER	
LEADER, WILLIAM T	

ART UNIT	PAPER NUMBER
1742	10

DATE MAILED: 10/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,911	WANG, HUI	
	Examiner	Art Unit	
	William T. Leader	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *110-118* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *110-118* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 110-116 and 118 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al (5,882,498) in view of Fairbairn et al (6,176,667).

3. The Dubin et al patent is directed to the production of semiconductor wafers. During the production of the wafer a number of processes are carried out. These include a step of electroplating and a spin/rinse/dry step. Dubin et al disclose that after a metal layer is formed during the electroplating process, the silicon substrate is removed from the electrolyte solution and transferred to another process chamber such as a spin/rinse/dry chamber (column 1, lines 56-60>

4. Dubin et al is silent as to the manner in which the chambers are positioned and the way in which the wafers are moved between chambers. Independent claim 110 and 113 differ from Dubin et al by reciting stacked modules and a transferring mechanism. The Fairbairn et al patent is directed to a wafer processing system. Fairbairn et al disclose that floor space in a clean room used for fabricating semiconductor devices is expensive. The per-square-foot construction cost, as well as maintenance cost, is high (column 1, lines 28-30). To reduce the amount of floor

space required, thereby lowering capital cost per wafer processed, Fairbarin et al propose stacking processing chambers one above another vertically (column 1, lines 50-55). As shown in figure 1, wafers are removed from wafer cassette 12 by robot arm 32 and placed in processing chambers A1 and A2. While figure 1 shows two stacked chambers, Fairbarin et al teach that as many as desired may be stacked vertically (column 3, lines 17-18).

5. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have utilized stacked process chambers with a robot arm to transfer wafers as taught by Fairbarin et al to carry out the processes of plating and spin/rinse/drying disclosed by Dubin et al because less floor space would have been required, lowering the cost of producing the wafers. Claim 115 recites that the transfer mechanism includes a telescoping member movable with three degrees of freedom. As shown in figures 1 and 2 of Fairbarin et al, robot arm 32 is movable in the X-Y plane and is capable of telescoping to position the wafers in the processing chambers. Fairbarin et al disclose that the robot arm is lifted to pick up the wafers from the cassette (column 3, lines 48-51). This movement is in the Z direction, showing that the arm can move with three degrees of freedom. Figure 1 suggests that the robot actuator 33 which moves arm 32 in Fairbarin et al is mounted on a bottom portion of the frame as recited in instant claim 117. The provision of a second set of plating baths as

recited in instant claim 118 would have been obvious in view of the teaching of Fairbarin et al that as many chambers as desired may be vertically stacked.

6. Claim 117 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al (5,882,498) in view of Fairbarin et al (6,176,667) as applied to claims 110-114 and 118 above, and further in view of Davis (6,477,440).

7. Claim 117 recites that the transferring mechanism is mounted on a top portion of the frame. As noted above, in Fairbarin et al the transferring mechanism is mounted on a bottom portion of the frame. The David patent is directed to a method and apparatus for treating semiconductor wafers. A plurality of stacked chambers is provided. Transfer mechanism 52 is mounted on a shelf toward the upper portion of the frame. It would have been obvious at the time the invention was made to have mounted the transfer mechanism of a semiconductor processing apparatus in any position, such as a top portion of the apparatus frame as in Davis, from which the wafers could be transported to the various loading and processing chambers.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hirose (5,762,745) discloses wafer processing apparatus with stacked processing chambers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 703-308-2530. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 703-308-1146. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

WL
William Leader
September 29, 2003

ROY KING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700